AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF THE CLAIMS:

1. (original) A memory module including a non-volatile memory, a dynamic random access memory, a static random access memory and a control circuit that accesses the non-volatile memory, the dynamic random access memory and the static random access memory, comprising:

a dynamic random access memory interface for accessing the dynamic random access memory from a device outside the memory module; and

a static random access interface for accessing the static random access memory.

2. (original) A memory module according to Claim 1, wherein:

immediately after power is turned on, data in a predetermined address region of the non-volatile memory is transferred to the static random access memory.

3. (original) A memory module according to Claim 1, wherein:

immediately after power is turned on, data in a predetermined address region of the non-volatile memory is transferred to the dynamic random access memory.

4. (original) A memory module according to Claim 1, wherein:

data transfer between the non-volatile memory and the dynamic random access memory is performed according to an instruction via the dynamic random access memory interface.

5. (original) A memory module according to Claim 1, wherein:

data transfer between the non-volatile memory and the static random access memory is performed according to an instruction via the static random access memory interface.

6. (original) A memory module according to Claim 1, wherein:

in data transfer from the non-volatile memory to the static random access memory or the dynamic random access

memory, data acquired by correcting an error is transferred.

7. (original) A memory module according to Claim 1, wherein:

in data transfer from the static random access memory or the dynamic random access memory to the non-volatile memory, an address replacement process is executed.

8. (original) A memory module according to Claim 1, wherein:

a boot program is held in the non-volatile memory.

9. (original) A memory module according to Claim 1, wherein:

data transfer range data showing a range of data transferred from the non-volatile memory to the dynamic random access memory at initial time when operating power is turned on is held in the non-volatile memory.

10. (original) A memory module according to Claim 1, wherein:

the non-volatile memory and the dynamic random access memory have the similar memory size; and

the static random access memory has memory size equal to/smaller than 1/1000 of that of the non-volatile memory.

Claim 11 (cancelled)

12. (original) A memory module according to Claim 1, wherein:

the data-hold operation of the dynamic random access memory is executed inside the memory module.

13. (original) A memory module according to Claim 11, wherein:

in case data-hold operation is instructed from the device outside the memory module to the dynamic random access memory, the data-hold operation of the dynamic random access memory inside the memory module is stopped.

14. (original) A memory module according to Claim 1, wherein:

access from the device outside the memory module is first preceded;

the data-hold operation of the dynamic random access memory inside the memory module is second preceded; and

data transfer between the non-volatile memory and the static random access memory or the dynamic random access memory is third preceded.

15. (original) A memory module according to Claim 1, wherein:

the dynamic random access memory is synchronous DRAM; and

access to the non-volatile memory and the dynamic random access memory from the device outside the memory module is made via an interface of the synchronous DRAM.

16. (original) A memory module according to Claim 1, wherein:

the non-volatile memory is a NAND flash memory; and

the dynamic random access memory is synchronous DRAM.

17. (original) A memory module according to Claim 1, wherein:

the non-volatile memory is an AND flash memory; and

the dynamic random access memory is synchronous DRAM.

18. (original) A memory module according to Claim 1, wherein:

the non-volatile memory performs error detection, error correction and address replacement.

Claims 19-20 (cancelled)

21. (original) A memory module according to Claim 1, wherein:

the dynamic random access memory is equipped with plural interfaces.

Claims 22-23 (cancelled)

24. (original) A memory module according to Claim 1, wherein:

the dynamic random access memory is equipped with a control circuit for processing access from the device outside the memory module and a control circuit for independently accessing the non-volatile memory.

25. (original) A memory module according to Claim 1, wherein:

the dynamic random access memory is equipped with a control circuit for independently accessing the non-volatile memory and a circuit for subordinately processing the access.

Claim 26 (cancelled)

27. (original) A memory module according to Claim 1, wherein:

the non-volatile memory is equipped with a static random access memory, an error detecting and correcting circuit and an address replacement circuit.

28. (original) A memory module according to Claim 1, wherein:

the non-volatile memory is equipped with plural interfaces.

Claims 29-78 (cancelled)